AMENDMENT TO THE CLAIMS

1. (Canceled)

2. (Currently Amended)   The adder based circuit of claim 1, including one or more ~~additional~~ elements coupled to at least one of the inputs of the input module and outputs of the output module ~~to~~ so that the circuit performs a ~~perform the~~ function selected from the group comprising subtractors, adder-subtractors, incrementors, decrementors, increment-decrementors and absolute value calculators.

3. (Currently Amended)   The adder based circuit of claim 2, wherein the ~~additional~~ elements are selected from the group comprising inverter elements, exclusive or elements, exclusive nor elements and multiplexers.

4. (Canceled)

5. (Canceled)

6. (Currently Amended)   The process of claim ~~5~~22, wherein the recursive functions are selected from the group consisting of $HV\_\{n-k\} = \{h'\_1,v'\_1,...,h'\_\{n-k\},v'\_\{n-k,\}\}$ and either (i) $H\_k = \{h\_1,..., h\_k\}$ or (ii) $HV\_k = h\_1,v\_1,...,h\_k,v\_k$ and $HV\_\{n-k\} = h'\_1,v'\_1,...,h'\_\{n-k\},v'\_\{n-k\}$, where $v\_k = V\_n]\&...\&V[n-k+1]$.

7. (Currently Amended)   The process of claim ~~4~~22, wherein the carry module includes negation elements and the process further ~~including steps~~includes a step of:
    c)   optimizing a distribution of ~~negations~~ negation elements in the carry module.

8. (Original)   The process of claim 7, wherein step (c)

comprises, for each portion of the carry module, steps of:
- c1) identifying a set of delay vectors,
- c2) recursively comparing the delay vectors to derive a set of minimum vectors, and
- c3) selecting a vector with a minimum norm from the set of minimum vectors.

9. (Currently Amended)   The process of claim ~~4~~22, further including a step of:
- c) minimizing a depth of the adder based circuit.

10. (Original)   The process of claim 9, wherein step (c) comprises:
- c1) recursively expanding expressions
  $DH\_n = \min\{\max(DH\_\{n-k\}+1, Dh\_k+2, DH\_k\}\}$ and
  $Dh\_n = \min\{\max(Dh\_\{n-k\}+1, Dh\_k+2\}\}$
  where DH_k and Dh_k are based on vectors of depths $U[i]$ for $0 \leq i \leq k-1$ and $DH\_\{n-k\}$ and $Dh\_\{n-k\}$ are based on vectors for $k \leq i \leq n-1$, and
- c2) selecting a value of k based on a minimum of at least one of DH_n and Dh_n.

11. (Original)   The process of claim 10, wherein step (c2) comprises steps of
  calculating vectors DHh_n based on maximum values of DH_n and Dh_n,
  sorting values of k to derive a set of minimum vectors DHh_n, and
  searching the set of minimum vectors to select a value of k.

12. (Currently Amended)   The process of claim ~~4~~22, further including a step of:
- c) minimizing fanout depth of the adder based circuit.

13 - 15. (Canceled)

16. (Currently Amended)   The storage medium of claim ~~15~~26,
wherein the recursive functions are selected from the group
consisting of $HV_{n-k} = \{h'_1, v'_1, \ldots, h'_{n-k}, v'_{n-k,}\}$ and
either (i) $H_k = \{h_1, \ldots, h_k\}$ or (ii) $HV_k =$
$h_1, v_1, \ldots, h_k, v_k$ and $HV_{n-k} = h'_1, v'_1, \ldots, h'_{n-k}, v'_{n-k}$,
where $v_k = V_n] \& \ldots \& V[n-k+1]$.

17. (Currently Amended)   The storage medium of claim ~~14~~25,
wherein the circuit structure defined by the processor includes a
carry module and further including third processor executable
instructions that enable the processor to optimize a distribution
of negation elements ~~negations~~ in the carry module, the third
processor executable instructions comprising:
  processor executable instructions that enable the processor
      to identify a set of delay vectors in each portion of
      the carry module,
  processor executable instructions that enable the processor
      to recursively compare the delay vectors in each
      portion to derive a set of minimum vectors, and
  processor executable instructions that enable the processor
      to select a vector for each portion with a minimum norm
      from the set of minimum vectors.

18. (Currently Amended)   The storage medium of claim ~~14~~25,
further including third processor executable instructions that
enable the processor to minimize depth of the adder base circuit,
the third processor executable instructions comprising:
  processor executable instructions that enable the processor
      to recursively expand expressions
      $DH_n = \min\{\max(DH_{n-k}+1, Dh_k+2, DH_k)\}$ and

Dh_n = min{max(Dh_{n-k}+1,Dh_k+2}}

where DH_k and Dh_k are based on vectors of depths U[i]

for $0 \leq i \leq k-1$ and DH_{n-k} and Dh_{n-k} are based on

vectors for $k \leq i \leq n-1$, and

processor executable instructions that enable the processor to selecting a value of k based on a minimum of at least one of DH_n and Dh_n.

19. (Original)   The storage medium of claim 18, wherein the computer instructions that enable the processor to select a value of k comprises:

processor executable instructions that enable the processor to calculate vectors DHh_n based on maximum values of DH_n and Dh_n,

processor executable instructions that enable the processor to sort values of k to derive a set of minimum vectors DHh_n, and

processor executable instructions that enable the processor to search the set of minimum vectors to select a value of k.

20. (Canceled)

21. (New)   An adder based circuit embodied in an integrated circuit comprising

an input module responsive to inputs A[i] and B[i] to generate a first input function U[i] = A[i]&B[i] and a second input function V[i] = A[i]$\lor$B[i] or V[i] = A[i]$\oplus$B[i];

a carry module responsive to the first and second input functions to generate carry functions; and

an output module responsive to the first and second input functions and the carry function to provide an output function

$$S = \sum_{i=0}^{n} 2^{i} S[i] \;=\; \sum_{i=0}^{n-1} 2^{i} A[i] \;+\; \sum_{i-0}^{n-1} 2^{i} B[i],$$

wherein the carry module has a minimal depth defined by a recursive expansion of at least one function associated with the carry module based at least in part on a parameter k, where k ≥ F_l and n-k ≤ F_{l-1} and where l satisfies F_l < n ≤ F_{l+1}, F_{l-1}, F_l and F_{l+1} are members of a Fibonacci series and n is the number of bits of at least one of the inputs.

22. (New)   A process of designing an adder based circuit for an integrated circuit comprising steps of:

    a)   defining an input module of the adder based circuit having an n-bit input;

    b)   defining at least one carry function of a carry module of the adder based circuit using conjunction elements; and

    c)   recursively expanding the carry function to find a minimum parameter, k, where k ≥ F_l and n-k ≤ F_{l-1}, l satisfies F_l < n ≤ F_{l+1}, and F_{l-1}, F_l and F_{l+1} members of a Fibonacci series.

23. (New)   The process of claim 22, wherein step (b) comprises steps of:

    b1)   defining recursive functions

        h'_l   =   h_l(U[k+1],U[k+2],V[k+2],...,U[k+1],V[k+1]) and

        v'_l = V[k+1]&,...,&V[k+1],

        where l = 1,...,n-k and U[i] and V[i] are inputs to the carry module, k = F_l and n-k = F_{l-1}, l satisfies F_l < n ≤ F_{l+1}, {F_l} is the

Fibonacci series defined recursively from the equality $F_{l+1} = F\{l\}+F_{l+1}$ and n is the number of bits of an input to the carry module, and

b2) recursively expanding the recursive functions to minimize l.

24. (New) The process of claim 12, wherein step (c) comprises steps of:

c1) defining recursive functions

$H^i_k = h^{i+1}_{k-1} \lor v^{i+1}_{k-1} \& h^i_l$

and

$v^i_l = v^{i+1}_{k^l} \& v^i_l$

based on a function of the adder based circuit, where k $= F_l$ and n-k $= F_{l-1}$, l satisfies $F_l < n \leq F_{l+1}$, $\{F_l\}$ is the Fibonacci series defined from the equality $F_{l+1} = F\{l\}+F_{l+1}$ and n is the number of bits of an input to the adder based circuit, and

c2) recursively expanding the recursive functions to minimize l.

25. (New) A storage medium having stored therein

first processor executable instructions that enable a processor to define an adder based circuit structure for an integrated circuit comprising elements that define at least one output function in terms of a Fibonacci series; and

second processor executable instructions that enable the processor to recursively expand the output function to find a minimum parameter, k, where k $\geq F_l$ and n-k $\leq$ F_{l-1}, l satisfies $F_l < n \leq F_{l+1}$, and F_{l-1},

F_l and F_{l+1} are members of a Fibonacci series.

26. (New)   The storage medium of claim 25, wherein the circuit structure defined by the processor includes a carry module and the second processor executable instructions comprises:

processor executable instructions that enable the processor to define recursive functions

$h'\_l = h\_l(U[k+1],U[k+2],V[k+2],\ldots, U[k+1],V[k+1])$ and

$v'\_l = V[k+1]\&,\ldots,\&V[k+1]$,

based on a carry function of the carry module, where k = F_l and n-k = F_{l-1}, l satisfies $F\_l < n \leq F\_{l+1}$, $\{F\_l\}$ is the Fibonacci series defined recursively from the equality $F\_{l+1} = F\{l\}+F\_{l+1}$ and n is the number of bits of an input to the carry module, and

processor executable instructions that enable the processor to recursively expand the recursive functions to minimize l.

27. (New)   The storage medium of claim 25, further including third processor executable instructions that enable the processor to minimize fanout depth of the adder base circuit, the third processor executable instructions comprising:

processor executable instructions that enable the processor to define recursive functions

$H^i\_k = h^{i+1}\_{k-1}\vee v^{i+1}\_{k-1}\&h^i\_l$

and

$v^i\_l = v^{i+1}\_{k^l}\&v^i\_l$

based on a function of the adder based circuit, where k = F_l and n-k = F_{l-1}, l satisfies $F\_l < n \leq F\_{l+1}$, $\{F\_l\}$ is the Fibonacci series defined from the equality $F\_{l+1} = F\{l\}+F\_{l+1}$ and n is the number of bits of

an input to the adder based circuit, and
processor executable instructions that enable the processor
to recursively expand the recursive functions to
minimize l.